ABSTRACT

The cache memory in the present invention includes a prediction unit 39 which predicts, based on the progress of the memory access outputted from the memory, a line address which should be prefetched next. The prediction unit 39 includes: a prefetch unit 414 which prefetches data of the predicted line data, from the memory to the cache memory; and a touch unit 415 which sets the predicted line address to the cache entry, as a tag, and validates the valid flag, without loading data from the memory into the cache memory.